REMARKS

This application has been amended so as to place it in condition for allowance at the time of the next Official Action.

The Official Action rejects claims 1-8 under 35 USC §103(a) as being unpatentable over IRIE 6,534,386 in view of SAKAMOTO et al. 2002/0028525. Reconsideration and withdrawal of this rejection are respectfully requested for the following reasons:

The Official Action offers the primary IRIE reference for all of the features recited in the rejected claims with the exception of the presence and use of alignment marks. It is this feature for which the secondary SAKAMOTO et al. reference is offered.

As is evident from the sequence drawing Figures 1A-1F, 4A-4E, and 5A-5E, each of the various embodiments of the IRIE method involves first slicing a wafer into respective chips, followed by flowing a layer of uncured resin onto the now-separated chips. Critically, as is apparent from Figures 1D, 4C, and 5E, the previously separated chips are spread apart from one another prior to the curing of the resin, thereby providing additional space between adjacent chips and leaving a resin covering for the sides of the chips.

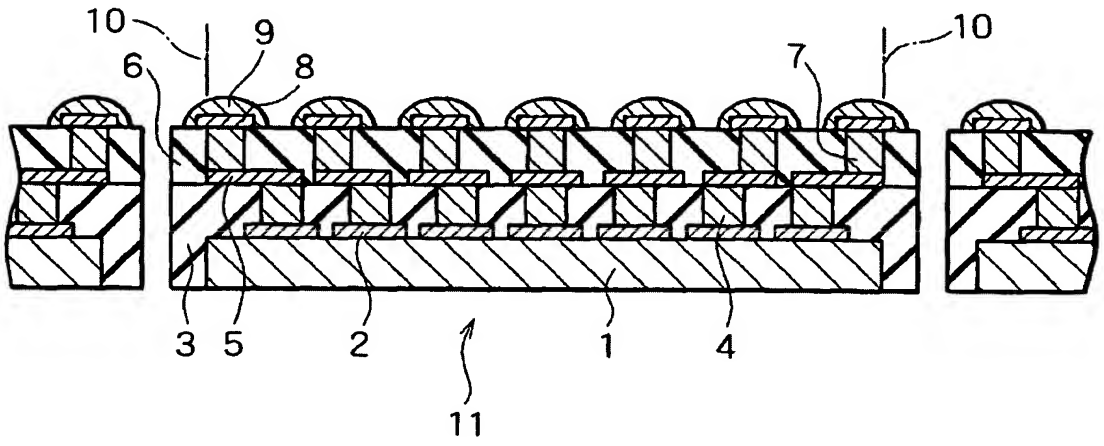
The sole purpose for the IRIE method is to overcome the shortcomings of the acknowledged prior art illustrated in Figures 7A-7D of such reference. As is illustrated therein, the prior

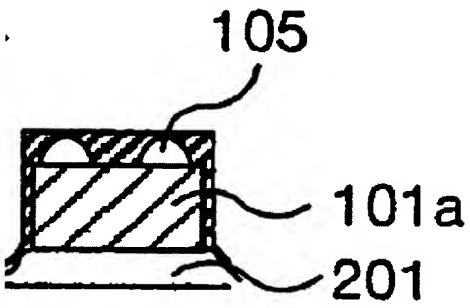
art method used two successive slicing steps illustrated in Figures 7B and 7D. In order to provide for a resin coating over the sides of the chips exposed during the first slicing, the second slicing of Figure 7D after curing of the resin must necessarily be of a narrower width than that of the first cutting in Figure 7B. As a result, if the second cutting of Figure 7D is performed with the narrowest width that the current technology allows, the previous cutting illustrated in Figure 7B necessarily uses sub-optimal cutting technology that removes a greater portion of the overall wafer than is necessary.

As a result of this motivation and resulting approach, the IRIE method offers nothing whatsoever in terms of providing a final chip package in which the electrical contacts for the package extend outside of the plan-view perimeter of the chip itself. For example, the sequence 5A-5E of IRIE includes bumps 105 as contacts. Significantly, each of such bumps lies entirely within the perimeter of the chip 101a.

In this regard, the present invention provides a striking contrast with the IRIE method and other known prior art. In the present method, a chip size package (CSP) is produced which maintains the benefits of a compact form factor while allowing for an array of contact pads for the final device that extends outside the perimeter of the chip itself. Present Figure 12 provides a useful sectional side view of the chip resulting from the present method. Figure 12 is reproduced below, together

with a portion of Figure 5E of IRIE, highlighting the layout distinctions therebetween.





As is evident from the two drawings, using the method of the present invention, the CSP pads 8 and CSP bumps 9 extend beyond the perimeter 10 of the LSI chip 1. In stark contrast, the bumps 105 of IRIE clearly lie within the perimeter of the chip 101a.

Applicant has amended independent claim 1, which now highlights the distinctions between the present invention and the disclosure of the prior art. Claim 1 recites the formation of at least wire layer with a corresponding resin layer, and the

subsequent formation of CSP pads on the wire layer resin. The chips are separated from one another by slicing through the cured resin layers. Moreover, claim 1 recites that from a plan view perspective of the CSP package, a perimeter of the resin lies outside that of the LSI chip. Additionally, at least one of the CSP pads extends outside the peripheral edge of the LSI chip.

As discussed above, and as readily illustrated by the comparison of the illustrated result of the present and prior art methods, neither the primary IRIE patent nor the secondary SAKAMOTO ET AL. patent serves to teach or suggest the features now explicitly recited in amended independent claim 1.

In addition to the amendments described above, applicant has added new independent claims 9 and 10. Each of these claims additionally recites a set of method steps for forming CSP type packages from a wafer using a sequence of steps that is neither disclosed nor suggested by any of the known prior art, including the IRIE and SAKAMOTO et al. references discussed above.

In light of the amendments provided above and the arguments offered in support thereof, applicant believes that the present application is in condition for allowance and an early indication of the same is respectfully requested.

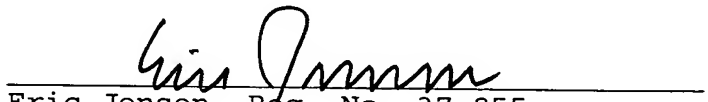
If the Examiner has any questions or requires further clarification of any of the above points, the Examiner may

contact the undersigned attorney so that this application may continue to be expeditiously advanced.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

YOUNG & THOMPSON



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